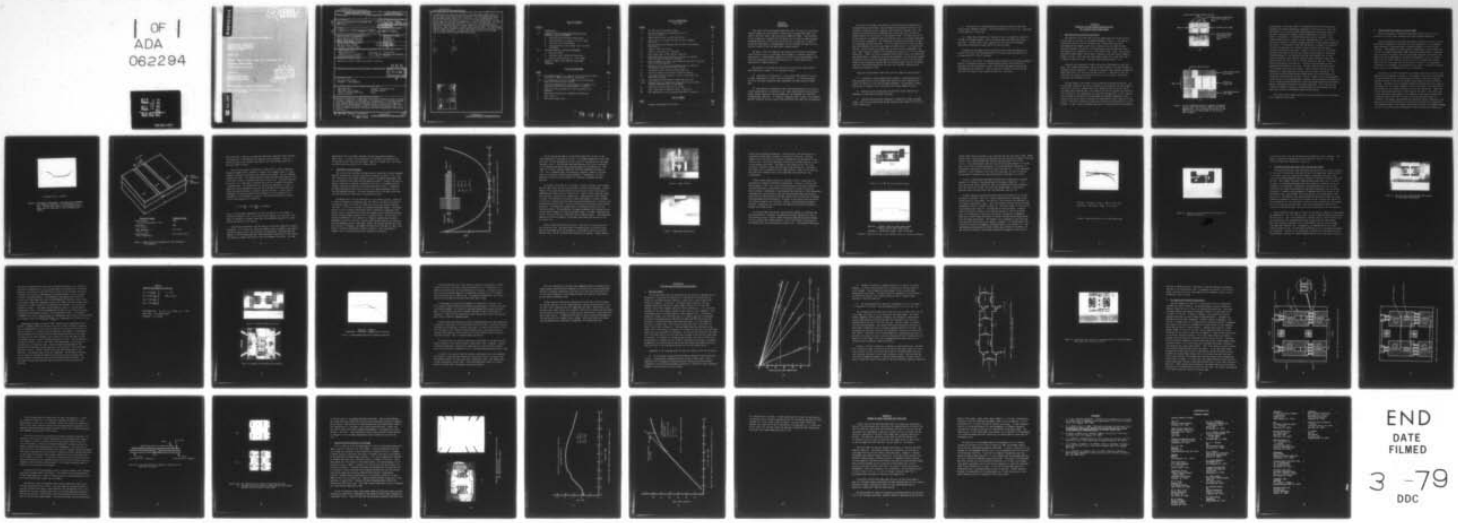
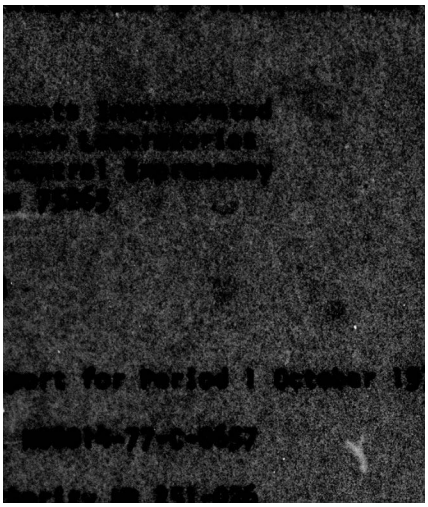
AD-A062 294 TEXAS INSTRUMENTS INC DALLAS CENTRAL RESEARCH LABS F/G 9/5
MONOLITHIC INTEGRATION OF MICROWAVE GAAS POWER FETS.(U)
OCT 78 V SOKOLOV, R E WILLIAMS, D W SHAW N00014-77-C-0657
UNCLASSIFIED TI-08-78-46 NL

| OF |
ADA
062294



END
DATE FILMED
3 -79
DDC



Unclassified

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER

2. GOVT ACCESSION NO.

3. RECIPIENT'S CATALOG NUMBER

4. TITLE (and Subtitle)

(6) MONOLITHIC INTEGRATION OF MICROWAVE GaAs POWER FETs,

5. TYPE OF REPORT & PERIOD COVERED

(9) Annual Technical Report, 1 October 1977 - 30 Sept 1978

6. PERFORMING ORG. REPORT NUMBER

(14) TI-08-78-46

7. AUTHOR(s)

(10) V. Sokolov, R. E. Williams and D. W. Shaw

8. CONTRACT OR GRANT NUMBER(s)

(15) N00014-77-C-0657

9. PERFORMING ORGANIZATION NAME AND ADDRESS

Texas Instruments Incorporated
Central Research Laboratories
13500 North Central Expressway
Dallas, Texas 75265

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS

PE62762N
RF-54-581-001
NR 251-026

11. CONTROLLING OFFICE NAME AND ADDRESS

Office of Naval Research
800 North Quincy Street
Arlington, Virginia 22217

(11) 12. REPORT DATE

October 1978

13. NUMBER OF PAGES

48

14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)

(16) F54581

(17) RF5458100 1

(12) 53p.

15. SECURITY CLASS. (of this report)

Unclassified

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited

DDC RECEIVED DEC 18 1978 B

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

ONR Scientific Officer:
Telephone: (202) 696-4218

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

GaAs Power FETs
GaAs Monolithic Circuits
Push-Pull Microwave Amplifier
Gallium Arsenide
Coplanar Transmission Lines
Microwave Devices
Baluns

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Monolithic integration of GaAs power field effect transistors (FETs) at X-band microwave frequencies is investigated. Incorporation of on-the-chip matching using lumped elements and coplanar ground metallization is investigated for monolithic FET device design. Coplanar microstrip transmission lines fabricated on alumina substrates are used to interface with the GaAs chips. Microstrip to coplanar microstrip transitions are also incorporated on the alumina substrate.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

403 833

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

To demonstrate the monolithic approach to microwave power amplification, a single-stage and two-stage push-pull amplifier were designed and fabricated. The two-stage design employs four transistors, a pair of 600 (μm) gate width devices for the first stage and a pair of 1.2 mm gate width devices for the second stage, monolithically integrated on a 2 mm x 2 mm GaAs chip. The single stage monolithic push-pull amplifier is just 1/2 of the two-stage chip. To provide the necessary 180° out of phase signals for the push-pull devices, 180° hybrid rings fabricated on alumina substrates are used. The single stage push-pull amplifier exhibits a small signal gain of 8 dB at 9.5 GHz with a 10% 1 dB fractional bandwidth. This amplifier yields 760 mW with 4.7 dB gain, also at 9.5 GHz with 21% power-added efficiency.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS

(continued)

LIST OF TABLES

SECTION I
INTRODUCTION

This report covers the progress made during the first year of a continuing research program for the monolithic integration of microwave GaAs power field effect transistors (FETs) under Contract No. N00014-77-C-0657. The objectives of this program are to demonstrate the feasibility of monolithic GaAs microwave integrated amplifier circuits utilizing power FETs in X-band and to identify significant advantages (or disadvantages) that this approach may have over the discrete transistor case for amplifying microwave signals.

The goal for the first phase of the program was to fabricate and evaluate a pair of power FETs on a single GaAs chip arranged in a push-pull amplifier configuration. Lumped element matching circuits were to be incorporated on the chip, thus avoiding the use of arched bond wires or flying leads for the realization of lumped inductances.

The purpose of the design and fabrication of a monolithic GaAs push-pull power amplifier for phase I of the program is twofold:

(1) The push-pull configuration is a very useful power amplifier circuit at lower frequencies for class A, AB, and B operation. It also has potential utility at microwave frequencies when implemented with GaAs monolithic power FETs.

(2) This amplifier configuration shows the advantage gained by the use of closely matched pairs of transistors (e.g., lower second harmonic distortion and greater dynamic range) and thus can demonstrate the advantage of a monolithic microwave power amplifier. It serves as a stepping stone to other, more versatile, matched transistor circuits, such as the differential pair amplifier configuration.

During the first phase, two monolithic FET mask sets were designed and corresponding devices fabricated. The first design incorporated an FET pair monolithically integrated with low impedance input and output coplanar lines. The purpose of this mask set was to generate device chips that could be used for characterization of the FET pairs in the push-pull mode. The chips also served as test vehicles for addressing the unique device and circuit problems associated with monolithic integration. The second mask set design incorporates four FETs in a two-stage push-pull amplifier. The first stage consists of a pair of 600 μm gate width devices, while the second stage includes a pair of 1.2 mm gate width devices. Series inductors and capacitors are monolithically integrated on the chip. Shunt inductors, however, are realized with bonding wire for initial design flexibility. (They, too, may be integrated monolithically once a firm design has been established.) In addition to the device development, microstrip and coplanar microstrip circuits were also designed and optimized for use as input and output networks that provide the required 180° out-of-phase signals (and also recombine them) for interfacing the push-pull FET pairs with standard unbalanced 50 Ω microstrip transmission lines.

Among the accomplishments made during the first phase are the following:

- A monolithic single stage push-pull amplifier incorporating a pair of 600 μm devices (half of the two-stage chip) exhibited a small signal gain of 8 dB at 9.5 GHZ with a 10% 1 dB fractional bandwidth. This amplifier yielded 760 mW with 4.7 dB gain, also at 9.5 GHZ with 21% power-added efficiency.

- Fabrication and incorporation of monolithic series inductors and capacitors on GaAs semi-insulating substrates.

- Improved device mounting techniques for handling of larger area GaAs chips. (The first and second mask designs had device chip areas of 9.7 mm^2 and 4 mm^2, respectively.)

- Fabrication of a two-stage monolithic push-pull amplifier employing lumped element impedance matching. The chip dimensions are 2 mm x 2 mm. Evaluation of this amplifier is under way.

- Design and optimization of interface circuits on alumina for realizing the 180° out-of-phase signals. Both a microstrip balun and 180° hybrid rings were used. The 180° hybrid rings, together with the microstrip-to-coplanar transitions, exhibited an excess loss of 0.4 dB at 9.5 GHz.

Although the two-stage monolithic amplifier had not been evaluated at the time of this report, the performance goal for this four-transistor amplifier is an output power of 1.5 W at 10 dB gain.

The rest of this report is organized basically around the two mask set designs. Section II discusses the FET pair characterization device, while Section III discusses the results obtained to date on the second chip design involving the two-stage push-pull amplifier. Finally, Section IV presents conclusions drawn from the first phase of this program and plans for future work.

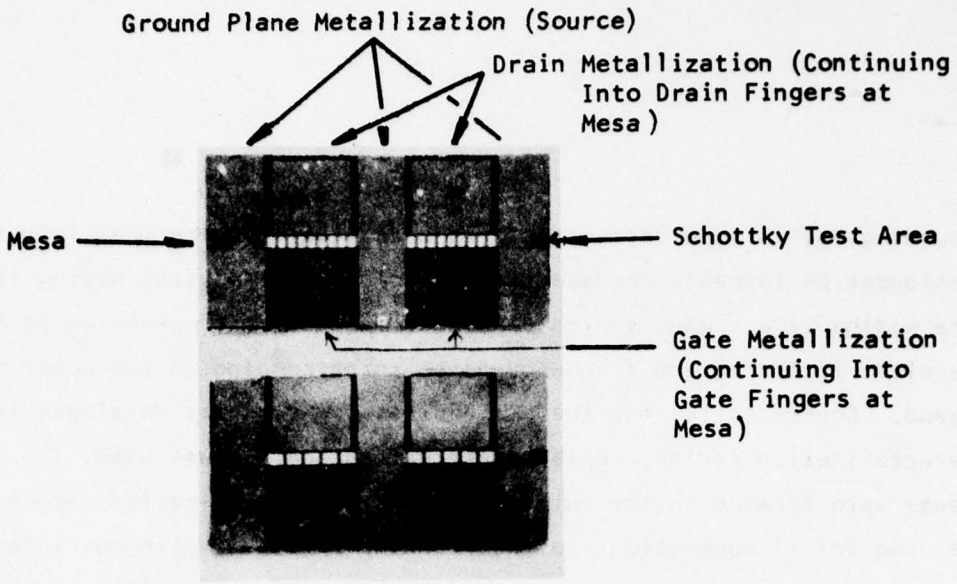
SECTION II
MONOLITHIC FET-PAIR CHARACTERIZATION DEVICE AND INTERFACE CIRCUIT DEVELOPMENT

A. Mask Description and Device Fabrication

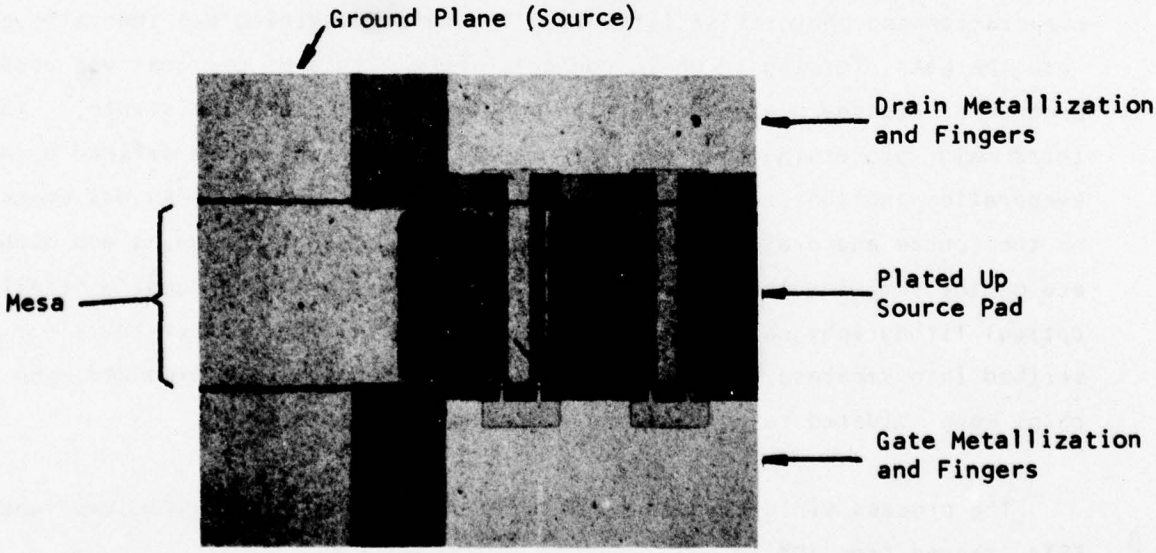
The monolithic structures that were fabricated using the initial characterization mask set are shown in the photomicrographs of Figure 1. The mask set produced two basic structures, differing only in gate width, which were simultaneously fabricated on each slice. Each structure included two FETs, associated coplanar transmission line metallization, and two Schottky barrier test patterns, all located on a 2.2 x 4.4 mm (86 x 174 mil) chip. One structure contained 32 gate fingers (150 μm each), yielding a total gate width of 4800 μm (2400 μm per FET); while the other had 16 gate fingers for a total gate width of 2400 μm (1200 μm per FET). The gate length was approximately 1 μm.

Since the two transistors of each structure are fabricated very near each other, their operating parameters should be nearly identical and thus suitable for balanced, push-pull operation. Yield was an important factor because one defective gate finger would ruin the entire two-FET structure. It was mainly this consideration that caused the 16-finger structure to be included in the mask set along with the 32-finger structure.

Coplanar geometry was chosen to allow convenient grounding of each FET. Our discrete FET transistors are usually grounded by stitch bonding the source pads on the FET chip with 25 μm diameter gold wire, extending these wires over the FET chip edge, and connecting them to the copper block carrier (ground) onto which the chip is soldered. For development of a monolithic FET amplifier circuit, however, this technique of grounding is not acceptable at microwave frequencies, since access to the carrier block is generally not available for every transistor of the circuit if the use of excessively long runs of source wire interconnects is to be avoided. In fact, there is evidence that even for discrete devices this method of



(a)



(b)

Figure 1 (a) Two Completed Monolithic, Coplanar Structures Having a Total Gate Width of 4800 μm and 2400 μm, Respectively. (b) A Close-Up View of Part of the 4800 μm Structure Showing Some of the Gate and Drain Fingers.

grounding may in some cases result in undesirable source lead inductance and consequent performance degradation, especially for devices having large total gate widths (i.e., many source pad interconnects) and operating at high frequencies, including the frequency range corresponding to the upper half of X-band. Consequently, for the FET devices and circuits developed in this characterization period, coplanar circuit technology was used, i.e., ground planes were located on the chip's surface, and the so-called coplanar waveguide[1] was used for rf connections to and from the devices. Although interconnection of the source pads was still required, access to ground was more readily available with coplanar techniques. Except for the inclusion of the coplanar grounding metallization over the semi-insulating GaAs substrate, the process already developed for the fabrication of GaAs power MESFETs[2] was utilized. After the epitaxial layer had been thinned by anodic oxidation, mesas were etched through the thin n layer to the semi-insulating substrate. The second step was source/drain metallization. The pattern was delineated by metal evaporation and photoresist lift-off. The metal remaining was then alloyed into the GaAs, forming an ohmic contact. AuGe with a Ni overcoat was used because of its sharp edge definition and very low contact resistance.[2] The third major processing step was gate metallization, which was defined by Al evaporation and photoresist lift-off. Finally, a layer of Cr/Au was evaporated on the source and drain bonding pads to improve current spreading and bondability, and on the semi-insulating substrate to form the coplanar grounding metallization. Optical lithography was used for all pattern definition. After the slice was scribed into separate structures, the source pads were stitch-bonded, and the chips were soldered to gold-plated copper mounting blocks.

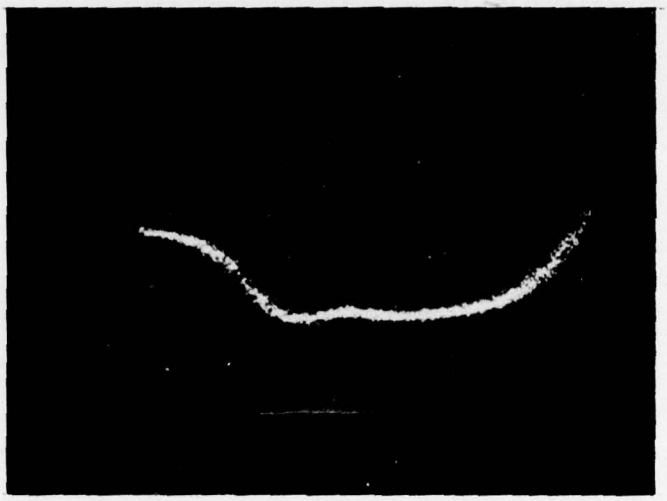
The process yield of good monolithic structures, each having two functional FETs, ranged from 30% to 60%.

B. Characterization of Passive Circuits on GaAs

Because the coplanar transmission lines were an essential part of the monolithic structure, their characteristics were studied independently.

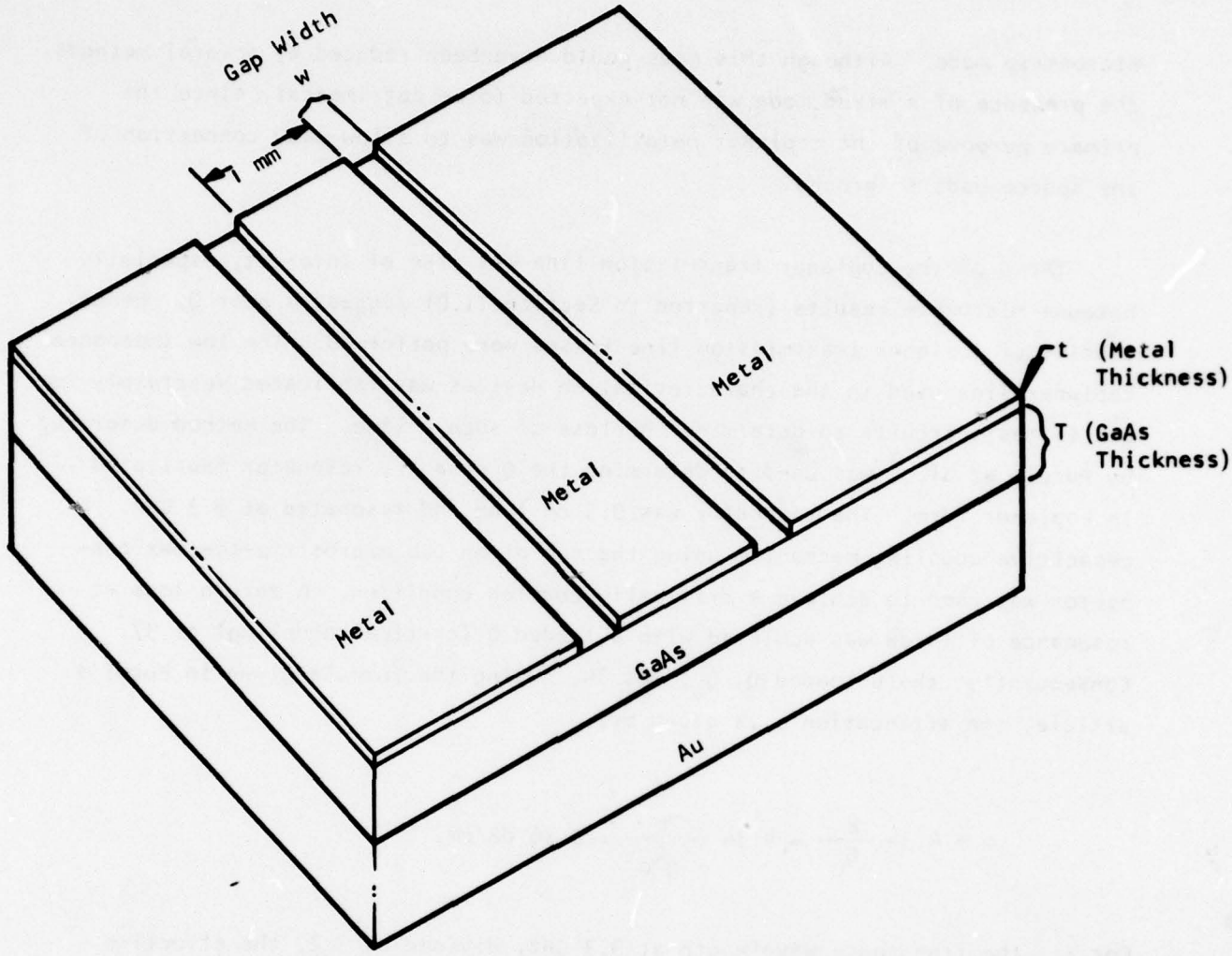
Coplanar transmission lines were fabricated on substrate material to allow experimental assessment of the effect of various parameters on line impedance. These parameters included gap width, substrate thickness, and metallization thickness. The impedances of these coplanar transmission lines were determined using a time domain reflectometer (TDR), which permits measurement of impedance as a function of time delay, and thus of distance, along the transmission line. Results of such a measurement for a coplanar transmission line with a 1000 μm (39.5 mil) wide center conductor and 76 μm (3.0 mil) wide gaps fabricated on 400 μm (16 mil) thick GaAs substrate are shown in Figure 2. The measurement indicated a line impedance of approximately 20 Ω, which is suitable for matching a 50 Ω line to a low impedance FET via a $\lambda/4$ transformer.

The results of similar measurements on coplanar transmission lines of other geometries are summarized in Figure 3. The parameters that were varied included the type of metallization, the metallization thickness, the width of the gap between the center stripe and the coplanar ground planes, and the thickness of the GaAs. The absence of any impedance change when the gap width (w in Figure 3) was changed from 75 to 100 μm suggested that the transmission line mode was not purely coplanar, but probably included a "microstrip" mode as well. (Note that a metal ground plane was present on the bottom of the slice.) This effect was further evaluated by measurement of the impedance as the coplanar ground metallization on each side of the 1 mm center strip was reduced in width until, ultimately, the coplanar ground planes were completely removed, leaving only the center strip and the metallization on the bottom of the 90 μm thick GaAs slice. This complete removal of the coplanar ground plane resulted in an impedance change of only 6 Ω from the original configuration, thus confirming the presence of a



Horizontal Scale = 20 ps/div

Figure 2 Time Domain Reflectometer Trace Showing the Impedance of a Coplanar Transmission Line Approximately 1 cm Long. The left-hand scale is the reflection coefficient, and the right-hand is the corresponding impedance.



Parameter Changed	Impedance Change
Metallization CrAu → Alloyed AuGe/Ni + CrAu	None
Gap Width, w 75 → 100 μm	None
Metal Thickness, t 0.6 → 1.1 μm	12 Ω → 9 Ω
GaAs Thickness, T 400 → 120 → 80 μm	21 Ω → 15 Ω → 12 Ω

Figure 3 Effect of Various Parameters on the Transmission Line Impedance

microstrip mode. Although this mode could have been reduced by several methods, the presence of a mixed mode was not expected to be detrimental, since the primary purpose of the coplanar metallization was to allow easy connection of the source pads to ground.

The Q of the coplanar transmission line was also of interest, especially because microwave results (reported in Section II.D) suggest a poor Q. Hence, studies of coplanar transmission line losses were performed. The low impedance coplanar line used in the characterization devices was fabricated separately for use in test circuits to determine the loss of such a line. The method described by Pucel, et al.,[3] was used to determine the Q of a $\lambda/2$ resonator fabricated in coplanar form. The resonator was 0.5 cm long and resonated at 9.3 GHz. A capacitive coupling mechanism using the tab of an OSM microstrip-to-coax connector was used to achieve a critically coupled condition. A return loss at resonance of 14 dB was achieved with a loaded Q (critical coupling) of 37. Consequently, the unloaded Q, Q_o, was 74. Using the formula given in Pucel's article, the attenuation α is given by,

$$\alpha \cong 4.34 \frac{\beta}{Q_o} = 4.34 \frac{2\pi}{\lambda_g Q_o} = 0.36 \text{ dB/cm.}$$

For λ_g, the free space wavelength at 9.3 GHz, divided by 3.2, the effective dielectric constant for the 1.0 mm (40 mil) wide coplanar line, was used. This value of 0.36 dB/cm is roughly three times the attenuation expected for a good quality microstrip line on alumina.

Work was also performed on the fabrication of monolithic capacitors on GaAs substrates. As it turned out, capacitive elements were not needed on the characterization devices used in the first part of the program. They were required, however, on the two-stage amplifier chips described in Section III of this report. The capacitive elements were metal-silicon nitride-metal structures. The lower

metallization was on the GaAs substrate, and the Si_3N_4 was approximately 5000 Å thick. In these initial experiments the top metal was defined on the nitride and did not cross over any edges. Capacitors ranging from 1 pF to 6 pF were fabricated and tested to 18 V without failure.

C. Interface Circuit Development

The circuits that interface the GaAs push-pull monolithic chip with standard OSM 50 Ω connectors must perform essentially two basic functions. First, they must transform an input signal originating from an unbalanced transmission line into two signals of equal amplitude and opposite polarity. Second, they need to effect a transition to coplanar transmission line so as to interface with the coplanar electrode configuration of the monolithic FET circuits. In addition, the above requirements must be met with a circuit design consistent with low loss and adequate bandwidth. Two such interface circuits are used, one at the input and the other at the output of the monolithic chip.

Two designs were initially developed for the interface circuits. The first is simply the analog of a waveguide magic tee, which in microstrip (coplanar or conventional) takes on the form of a 180° hybrid ring, more commonly called a "rat race." This circuit provides two unbalanced antiphase signals. The second type of circuit is a balun configuration which transforms an unbalanced transmission line to a balanced one in which both conductors are isolated from ground and can therefore feed a transistor pair in push-pull mode. One such balun is reported by DeBrecht,[4] but no analysis or frequency response data are given. Consequently, the first task was to perform this analysis based on the even and odd mode impedances given in that paper, compute the voltage standing wave ratio as a function of frequency, and compare the results with the 180° rat race. The result of the balun calculation is shown in Figure 4. Also illustrated in schematic form is the balun structure as realized in microstrip.

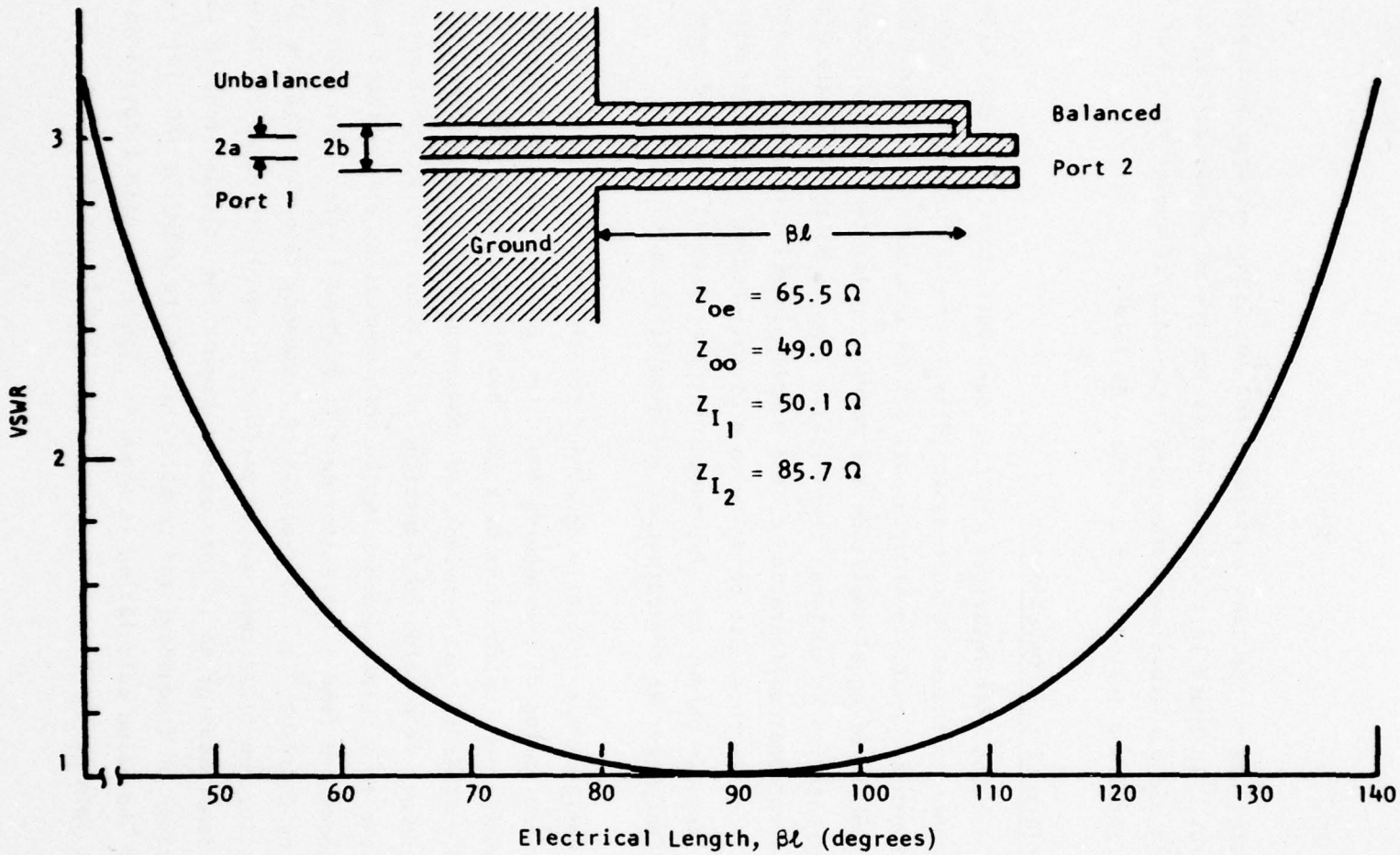


Figure 4 Theoretical Coplanar Balun Frequency Characteristic

The calculation was made for strip-width-to-gap ratio of about 11 and substrate-height-to-strip-width ratio of 1. The image impedance at center band ($\beta\ell = 90°$) for the unbalanced end is 50 Ω while for the balanced end the image impedance is 86 Ω. The VSWR was calculated assuming a 50 Ω source resistance at the unbalanced end and an 86 Ω load resistance at the balanced end. Note that for an octave frequency range (67% fractional bandwidth) the VSWR is 1.45. For a comparable VSWR, the theoretical frequency response of the 180° hybrid ring exhibits a 44% fractional bandwidth. Consequently, the balun approach is potentially more suitable for realizing a broadband push-pull amplifier.

To increase the chances for a successful low-loss interface circuit design, both the 180° hybrid and the microstrip balun circuits were developed. To date, however, more success has been achieved with the hybrid ring in the areas of repeatable performance and low insertion loss. Figures 5 and 6 show the etched balun and hybrid ring circuits, respectively. These were the initial designs. In Figure 5 the OSM coax to microstrip transition/connector is shown, attached to the circuit carrier block and contacting the conventional 50 Ω microstrip line. The coplanar section of 50 Ω line is in the center of the 0.63 mm thick alumina substrate. The three-strip coplanar balun is located at the bottom of the alumina substrate. The ground plane is brought up symmetrically through the two drilled holes by means of a 0.25 mm wide gold ribbon. To reduce inductance even further, the entire hole is filled with silver conductive epoxy. Three beam-lead capacitors (47 pF) are used for dc blocking, one at each hole and one at the 50 Ω input line.

Figure 6 shows the hybrid ring circuit. The input is at the left on the 50 Ω microstrip line. The hybrid ring is etched entirely in microstrip form. The two out-of-phase ports are brought out to the edge of the circuit via 50 Ω coplanar lines, and the transition from microstrip to coplanar is again made by

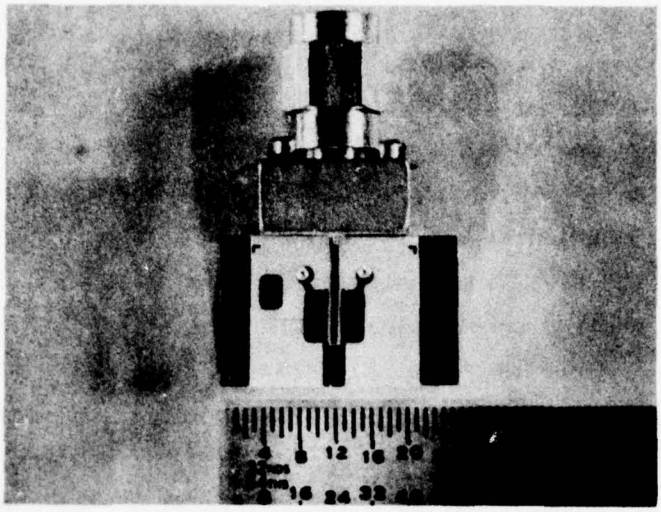


Figure 5 Balun Circuit

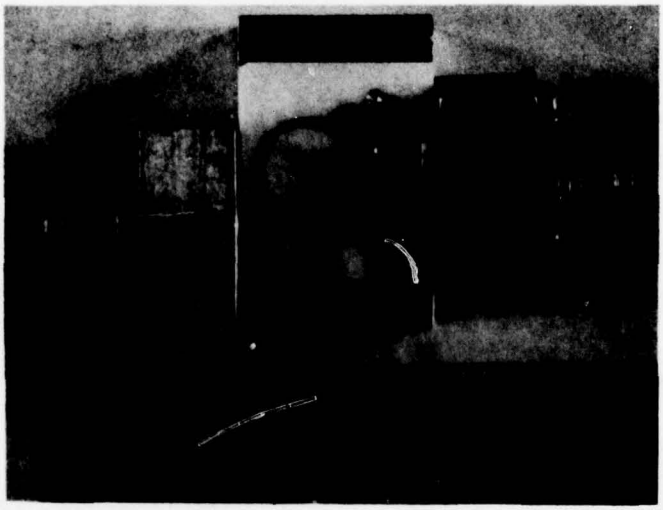


Figure 6 180° Hybrid Ring Circuit

holes drilled through the substrate. The fourth port, the isolated port, is terminated with 50 Ω and is evident in the center of the ring. Blocking capacitors were omitted in this version, although they are implemented in the final circuit. For initial evaluation of the circuit an OSM connector is used at the coplanar end as well. Also shown in the figure are two 100 Ω chip resistors in parallel, which terminate one of the output ports. The second 50 Ω output port is connected to the rf OSM connector. Both circuits have the two output ports adjacent so as to be compatible with the FET pair chip configuration.

After a second design iteration on the balun circuit, trouble was still encountered in obtaining satisfactory performance. Primarily, insertion loss was too high (~ 1 dB). Part of this problem was due to the abrupt termination of the ground plane on the bottom of the substrate at the 50 Ω microstrip/balun interface. Furthermore, it was observed that the electric field penetration underneath the microstrip balun into the 0.63 mm alumina substrate was quite significant and that the bottom interface conditions of the substrate influenced the performance quite significantly. A channel in the carrier block was milled, to provide a dielectric-air interface. However, poor performance was again observed. Resonances occurring within the channel and the alumina dielectric plagued this design as well.

On the other hand, the hybrid ring performance (except for bandwidth) was quite satisfactory. Therefore, this device was further optimized for use as the interface circuit. Figure 7 shows two hybrid rings connected back-to-back to form a two-way 180° divider/combiner. Gold straps connect the grounds and the coplanar 50 Ω lines associated with each circuit. The photograph shows gold

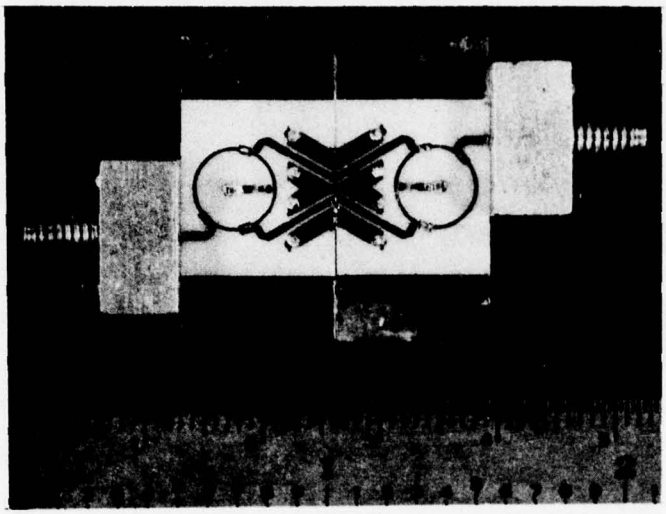
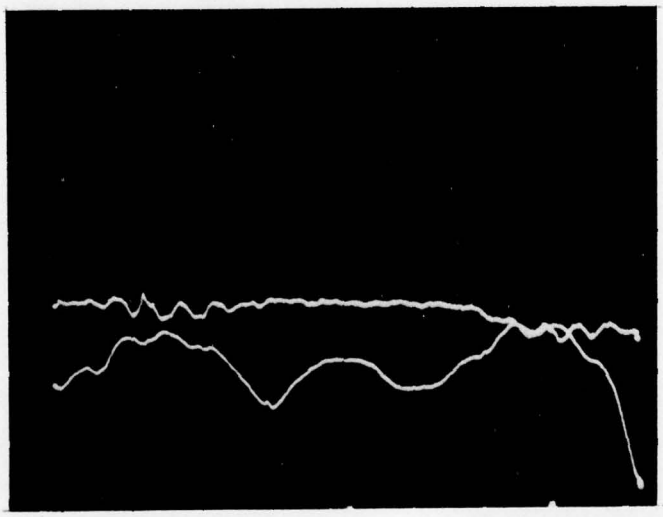


Figure 7 Two 180° Hybrid Rings Back-to-Back



Vertical: 1 dB/div (Insertion loss, upper trace)
10 dB/div (Return loss, lower trace)

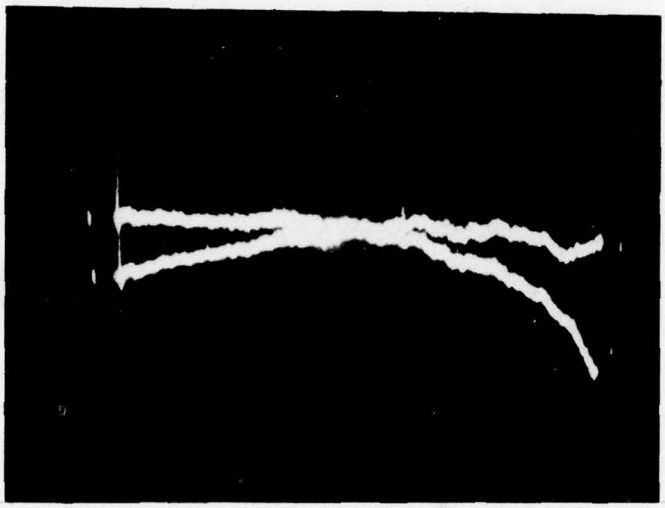
Horizontal: 250 MHz/div; Range: 8.25 → 10.75 GHz

Figure 8 Insertion and Return Loss Characteristics for Circuit of Figure 7

tuning straps, which are welded to the rings near the input and output lines. These straps tune out the discontinuity associated with the junctions of the 50 Ω lines and the 71 Ω ring. Figure 8 shows the insertion loss and return loss of this circuit. At 9.5 GHz a total insertion loss (for the divider/combiner) of 0.8 dB and a return loss of 18 dB are observed. For both hybrids the fourth port is terminated at the center of the ring by a 50 Ω chip resistor. A 10 pF beam-lead capacitor is also included in this line for dc blocking. As seen in Figure 8, the optimized rings have a very good characteristic from about 9 to 10 GHz.

Finally, Figure 9 shows the phase characteristic as measured on a network analyzer for the hybrid ring design used in the push-pull amplifier. It is seen that the two output signals are 180° out of phase with a phase tracking of ±5° from 8.4 GHz to 11.2 GHz. For this final design [seen in the push-pull amplifier photo of Figure 22(a)] the rings have mean radii of 3 mm.

Another important design accomplishment was the fabrication of a low loss microstrip-to-coplanar transition. Several approaches were undertaken during the early part of the program. The quality of the transition was measured by a time domain reflectometer system. One of the simplest designs, and yet one that yielded good results, is shown in Figure 10. The circuit shown is a test circuit for evaluating the transition. The substrate is 0.63 mm alumina. A ground plane on the bottom surface of the substrate extends over the entire bottom area. All transmission lines have a nominal 50 Ω characteristic impedance. Holes are drilled through the ceramic to connect the upper ground metallization with the bottom ground plane. The coplanar line is tapered in such a way that the transition from microstrip to coplanar is gradual. At the beginning of the transition the mode of propagation corresponds mostly to microstrip, i.e., the top coplanar ground planes are placed farther away and have little effect. At the end of the transition the coplanar dimensions correspond to nearly a 50 Ω



Vertical: 10 deg/div; Offset: 180° for "R" Trace
Horizontal: 400 MHz/div; Range: 8 to 12 GHz

Figure 9 Phase Characteristic for 180° Hybrid Ring

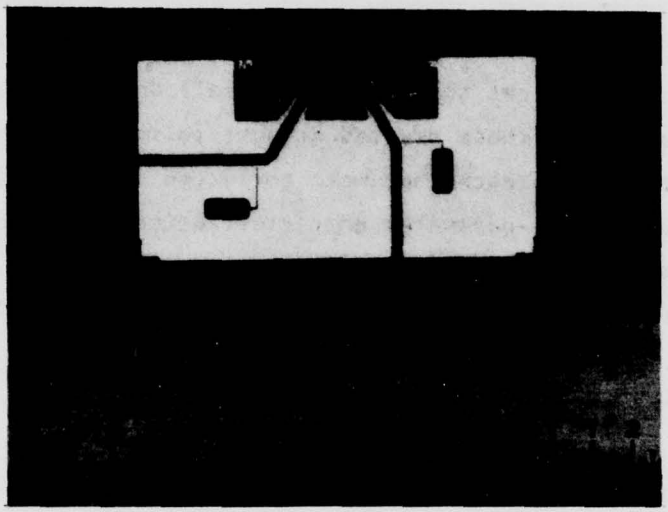


Figure 10 Test Circuit for Evaluation of Microstrip to Coplanar Transition

line (a/b ratio of ~ 0.5) and the bottom ground plane has little influence. Time domain reflectometer measurements show the transition results in a voltage reflection coefficient (magnitude) of about 0.1.

D. Findings and Conclusions Drawn from First Mask Set Design

The monolithic FET pair chips fabricated from the first mask set were intended for use primarily as devices to be used for small and large signal characterization. In retrospect, work with these devices brought to focus some very basic flaws in the initial design approach that were corrected in the second push-pull amplifier mask set. Small signal S-parameter characterization was done on the 1.2 mm pair FET chips, but accurate measurements were quite difficult to make due to the low impedance levels observed. Consequently, the measurements could not show the differences that might exist between the new device S-parameters (due to coplanar grounding, for example) and S-parameters of comparable gate width devices of the conventional type. Nevertheless, within the accuracy of the measurements, they did point out the important fact that the design of the push-pull amplifier could be based on S-parameters obtained from discrete devices, provided some flexibility was incorporated into the chip design to allow for minor differences in the characteristics of the new monolithic FETs. The following paragraphs summarize the results and conclusions drawn from the work with the devices of the first mask set.

Using the hybrid rings shown in Figure 7 of the previous subsection, S-parameters were measured for the 1.2 mm FET pair chip. Figure 11 shows the chip mounted between the two circuits. One of the properties of the 180° hybrid is that if both of the out-of-phase ports are terminated with equal voltage reflection coefficients, then that reflection coefficient will be translated to the input port through a fixed phase and insertion loss. Consequently, by compensating for this fixed insertion phase and loss, the reflection coefficient at the circuit/device interface can be measured. Similarly, the transmission coefficient for the device can also be determined. Using an H.P. network analyzer system, the circuit shown in Figure 7

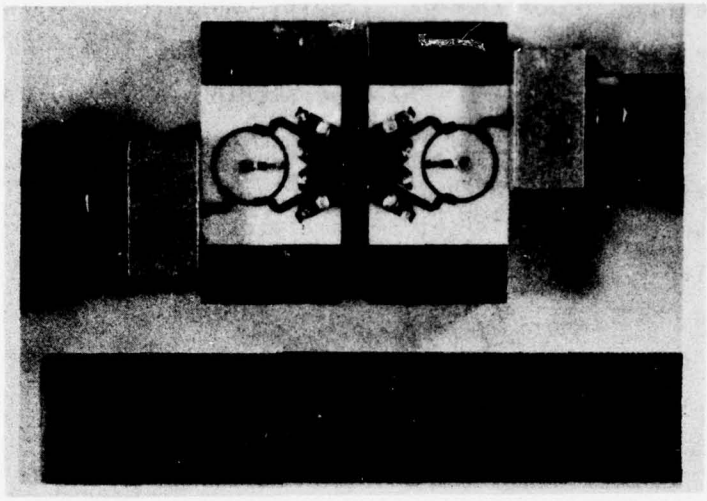


Figure 11 FET Pair Chip Mounted Between 180° Hybrids for S-Parameter Measurements

was used to established the "short" and "through" calibrations. For the "short" calibration (necessary for S_{11} and S_{22} measurement) the coplanar 50 Ω lines were shorted at the junction of the two circuits, while for the "through" calibration (necessary for S_{12} and S_{21} measurements) the divider/combiner circuit as shown in Figure 7 was used directly. The S-parameter measurements were restricted to the 9 to 10 GHz range due to the limited bandwidth of the hybrid rings. Over this frequency range the S-parameters varied only slightly (within the measurement uncertainty) so that a single set of parameters was recorded. The results are presented in Table 1. Also shown are the stability factor, k, and the maximum available gain, MAG. It should be emphasized that MAG is very sensitive to $|S_{11}|$ and $|S_{22}|$ and thus depends strongly on the measurement accuracy. For example, a change of only -0.01 in $|S_{22}|$ ($|S_{11}|$) will change MAG from 7.8 dB to 6.2 dB (6.8 dB), or a change of -0.01 in both $|S_{11}|$ and $|S_{22}|$ will change MAG from 7.8 dB to 5.5 dB.

Because $\angle S_{11}$ and $\angle S_{22}$ are close to 180°, single-section transformers incorporated in coplanar form into the hybrid ring MIC circuits of Figure 7 should be able to impedance-match to the input and output of the FET pair and result in a push-pull amplifier. To achieve the low impedance, the coplanar λ/4 transformers were fabricated on the alumina substrate and incorporated 0.05 mm (2 mil) gaps. To achieve an even lower impedance level, dielectric overlay was used over the λ/4 coplanar section. Figure 12 shows the amplifier circuit. The four dielectric overlays are seen as an "X" in the middle of the photograph. Tuning chips are also seen next to the hybrid rings. Figure 13 shows an enlargement of the device/circuit interface with the dielectric overlay removed. The 0.05 mm gaps are barely visible. Finally, Figure 14 shows the small-signal gain of this amplifier. At 9.25 GHz a gain of 4.5 dB is obtained. The horizontal reference line in Figure 14 includes the insertion loss of one of the two coaxial bias tees (not shown in the photos) used to bias the FET push-pull amplifier. The 4.5 dB gain includes the insertion loss of two hybrid ring circuits and one bias tee.

Table 1

Measured S-Parameters for FET Pair

$S_{11} = 0.9 \angle 165$

$S_{12} = 0.023 \angle -25$

$S_{21} = 0.25 \angle -35$

$S_{22} = 0.95 \angle -165$

$k = 1.18$

$MAG = 7.8$ dB

Bias Conditions : $V_D = 5$ V, $I_D = 419$ mA, $V_G = -1.00$ V

Device Pair: two 1200 μm FETs

Frequency: 9 to 10 GHz

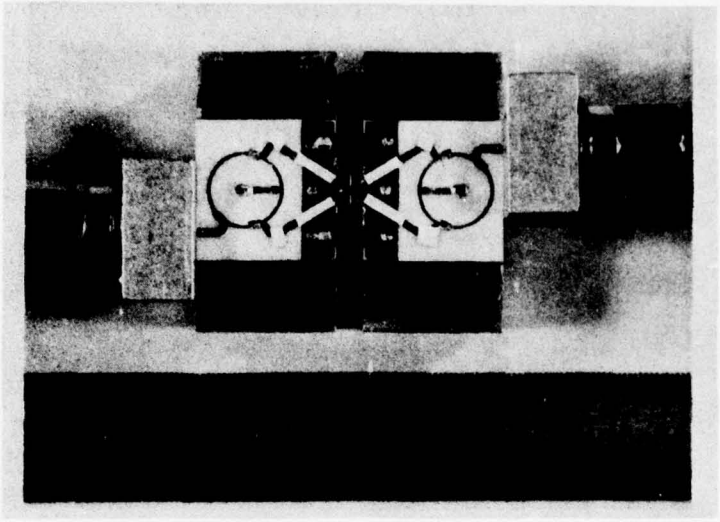


Figure 12 Push-Pull Amplifier Circuit

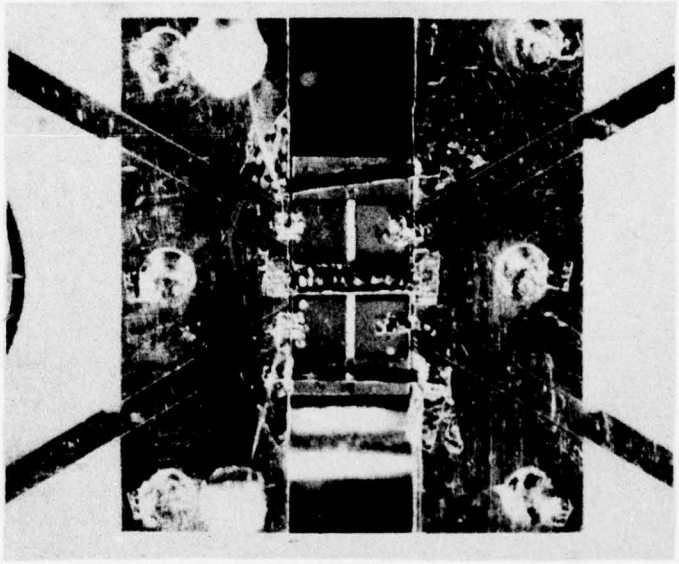
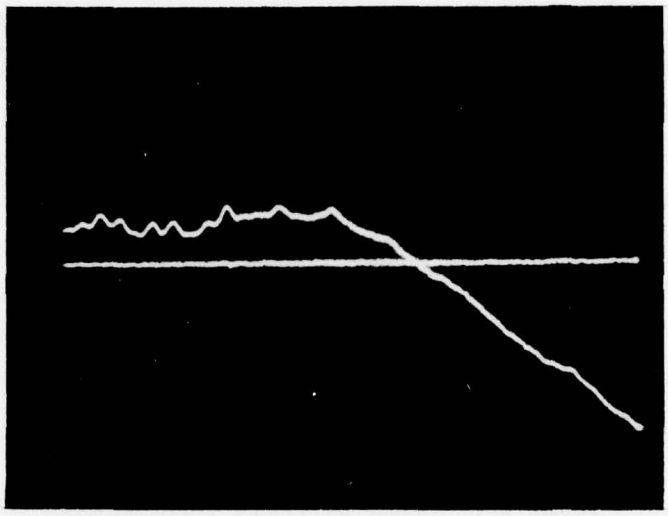


Figure 13 Details of Device/Circuit Interface



Vertical: 5 dB/div
Horizontal: 250 MHz/div; Range: 8.25 → 10.75 GHz

Figure 14 Small-Signal Gain of FET Push-Pull Amplifier

The above amplifier was further tested to assess its performance at larger signal levels and to evaluate an alternate matching circuit configuration for potential incorporation into the second amplifier mask set. Although low gains were a problem with this amplifier, we were able to obtain 0.5 W at 3 dB gain at 8.5 GHz using the 2 x 1200 μm chip. This amplifier consisted of the FET-pair characterization chip and the input and output hybrid rings.

An advantage of a push-pull arrangement of transistors is the fact that shunt matching elements may be used without the complication of having to dc-block for biasing purposes. An inductor is connected between the two gate (and drain) pads. Since effective ground is "between" the pads, a shunt configuration is achieved. In the 3 dB, 0.5 W amplifier a shunt inductor was used at the gate and drain pads to effect an impedance match.

Although both input and output circuits incorporated a quarter wave transformer in coplanar transmission line (transforming from 50 Ω to 18 Ω), this shunt inductor technique could be applied to matching the output of a 1200 μm FET directly to 50 Ω. This technique is more effective than a matching circuit incorporating series inductor/shunt capacitor series inductor (as is most commonly used for discrete FET power devices), since it conserves GaAs real estate.

The low gain was the result of excessively large areas for the gate and drain center conductor of the input and output transmission lines. Although, in theory, it should be possible to resonate this capacitance out with the shunt inductor, the Q of the monolithic transmission line is not high enough and causes loss in gain.

To confirm the suspicion that the coplanar transmission lines were degrading performance, a single FET was cleaved from a monolithic device in a manner that eliminated almost all the input and output transmission lines, thus leaving only a long, narrow gate or drain "pad." This device exhibited a gain of 6.7 dB at 9 GHz at the same (6 V) source-drain bias used previously.

From this experience it was clear that impedance matching techniques using lumped elements monolithically integrated on the chip were a promising approach, and that if coplanar transmission lines were to be used, they would need to be of much higher impedance to avoid unwanted capacitive coupling (to the bottom ground plane) and excessive loss.

Another important observation obtained with the devices of the first mask set was the realization of the unique mechanical problems associated with 0.1 mm (or less) thick, large area (9.7 mm^2) GaAs power FET chips. Specifically, chip cracking, poor solder joints, and in general, difficulty in working with the chips, was attributed to the necessity of requiring thin substrates for proper heat sinking of power devices. It emphasized the need for better mounting techniques and fixtures as well as for compact circuit design. Both these factors were taken into consideration and improvements implemented in the second mask set.

SECTION III
TWO-STAGE PUSH-PULL AMPLIFIER DEVELOPMENT

A. Amplifier Design

To more comprehensively test and demonstrate the monolithic approach to the development of GaAs power FET amplifiers, it was decided to proceed with the design of a two-stage push-pull amplifier, rather than a single stage as was originally proposed. In addition, a two-stage design simplifies the input impedance matching problem to the power stage by having a first stage that "absorbs" part of the impedance level drop from a nominal 50 Ω i.e., the output impedance of the first stage is generally lower than its input impedance. Thus, interstage matching is accomplished at a lower impedance level. Furthermore, because of a higher chip level power gain (a 10 dB gain amplifier is expected), the overall two-stage push-pull amplifier including the 180° hybrids has the potential for realizing a higher power-added efficiency, since the combining efficiency is higher than it would be for a lower gain chip. This effect is shown in the curves of Figure 15. The power-added combining efficiency versus excess loss in the divider (or combiner) is plotted with the gain of the individual amplifiers to be combined as the parameter. For the push-pull amplifier the excess loss in the 180° hybrid ring is 0.4 dB, while the gain is the intrinsic power gain of the chip. For example, by increasing the chip gain from 4 dB to 10 dB, a 10 percentage point increase from 79% to 89% in the combining efficiency is achieved. Consequently, for a 30% efficient device chip the overall power-added efficiency would be 23.7% for the 4 dB device and 26.7% for the 10 dB gain device.

Highlights of the two-stage push-pull amplifier design include the following.

- The chip design incorporates the essential elements of power monolithic circuits. Lumped element impedance matching is used to reduce size. Series capacitors for interstage dc blocking and series inductors are monolithically integrated. Bias distribution between transistors is realized by shunt inductance elements, which form part of the rf tuning.

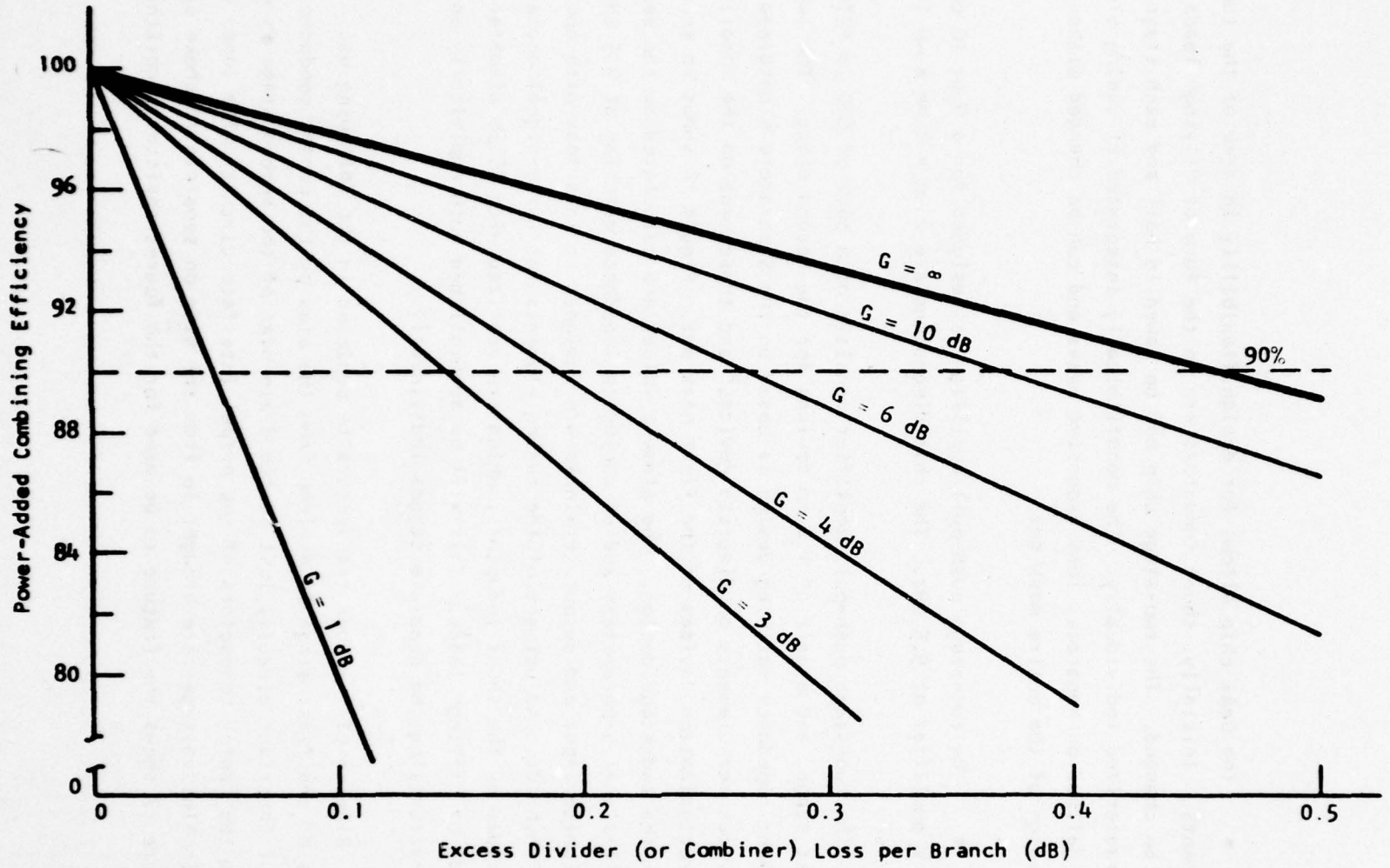


Figure 15 Added Power Combining Efficiency vs Divider (or Combiner) Loss with Amplifier Gain as a Parameter

- The GaAs chip allows for design flexibility in some of the tuning elements. Initially, shunt inductors are in the form of "flying" leads and can be changed. The two-stage chip can be sawed in half and each stage characterized individually. The monolithically integrated rf tuning elements are defined on separate, less expensive masks and can be changed without redesign of the entire mask set.

- The two-stage push-pull amplifier is designed for a 9 or 10 dB gain, 1.5 W amplifier at 9.5 GHz. The chip dimensions are 2 mm x 2 mm x ~0.1 mm.

The two-stage push-pull amplifier consists of a pair of 600 μm FETs for the first stage, and a pair of 1.2 mm devices for the second stage. The lumped element impedance matching design is based on the S-parameters obtained from previous measurements on discrete devices[5] and those made on the monolithic characterization devices of the first mask set. Figure 16 shows in schematic form the two-stage design. The element values are calculated on the basis of small-signal S-parameters and on conjugate impedance matching at 9.5 GHz. The antiphase input and output terminals are designed to interface with nominal 50 Ω 180° hybrids. Adjustment of the tuning elements for large-signal operation is provided by the shunt inductors, which are realized with 25 μm diameter gold wire bonds or "flying" leads. This will be accomplished both empirically and by characterizing the separate stages individually.

Biasing of the four transistors is achieved in the following way. The gate bias of the first stage is derived from the bias on the center conductors of the input interface circuit, just as the drain bias of the second stage is derived from the center conductors of the output interface circuit. The inner gate and drain bias voltages are brought in from the side on separate rf choke circuits. Figure 17 shows the fixture to be used for the four-transistor monolithic amplifier.

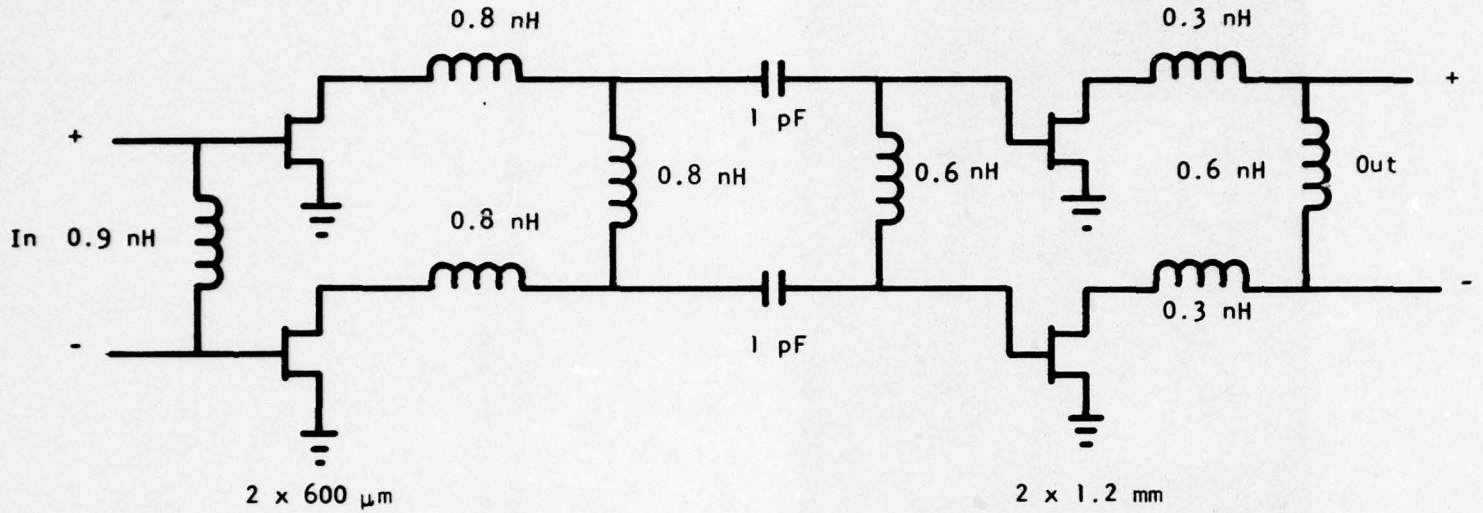


Figure 16 Design Schematic for Small Signal Monolithic Push-Pull Amplifier Chip for 9.5 GHz Operation

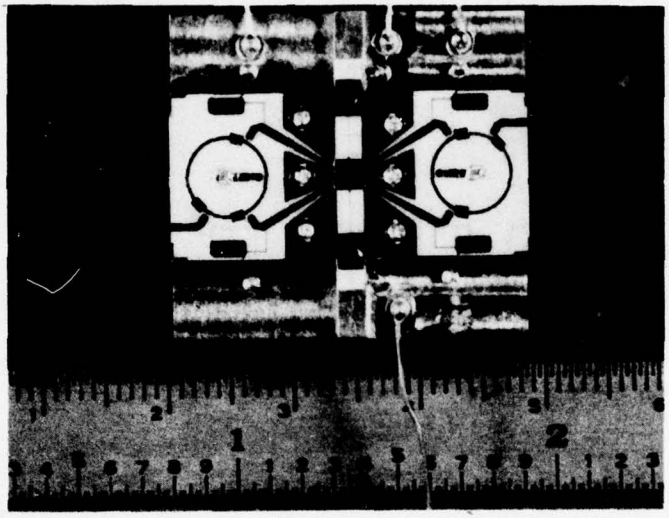


Figure 17 Microstrip Test Fixture for Two-Stage Push-Pull Amplifier Showing Bias Supply and Interface Circuits

The bias rf chokes are seen in the photo as lines of high and low impedance sections of $\lambda/4$ transmission lines. To suppress the possibility for low frequency oscillations, 0.01 μF chip capacitors are connected in shunt from the etched bias lines to ground.

B. Mask Description and Device Fabrication

The basic geometry of the 2.0 x 2.0 mm amplifier chip is schematically indicated in Figures 18 and 19. As discussed above, the shunt inductance elements (Figure 19) will initially be realized using gold wire. The series inductance elements and capacitive elements, however, are fabricated monolithically on the chip. A number of changes in the previous fabrication procedure were made to produce these two-stage amplifiers. The gates are defined by electron beam lithography, instead of optical lithography. This results in a higher yield of 1 μm gates than is obtained by optical lithography. The crosses in the center of the amplifier (Figures 18 and 19) are alignment marks that are used for e-beam alignment. The gate metallization is TiPtAu. Another change is the use of low-cost, computer-generated masks for several steps that do not require a high precision geometry. These include the printing of the series inductance elements. This allows these elements to be easily changed, since new masks can be generated quickly and at low cost. This mask set also produces a separate test area containing further e-beam alignment marks, a Schottky barrier for C-V profiling, gate resistance and contact resistance test patterns, and a gate recess pattern. This latter feature is used to improve slice yield and make the gate recess step easier. In the usual gate recess procedure the source-drain current is periodically checked during the etching procedure by forcing probes through resist to contact source and drain pads. This is more difficult with e-beam resist than with optical resist because the e-beam resist is harder. In either case, the probes sometimes slip and scratch across a gate area, thereby ruining one device and thus, in this case, one entire amplifier. These problems are eliminated in the present mask set by performing the probing on a separate pattern within the test area. This pattern has openings in the resist above the "source" and "drain" pads.

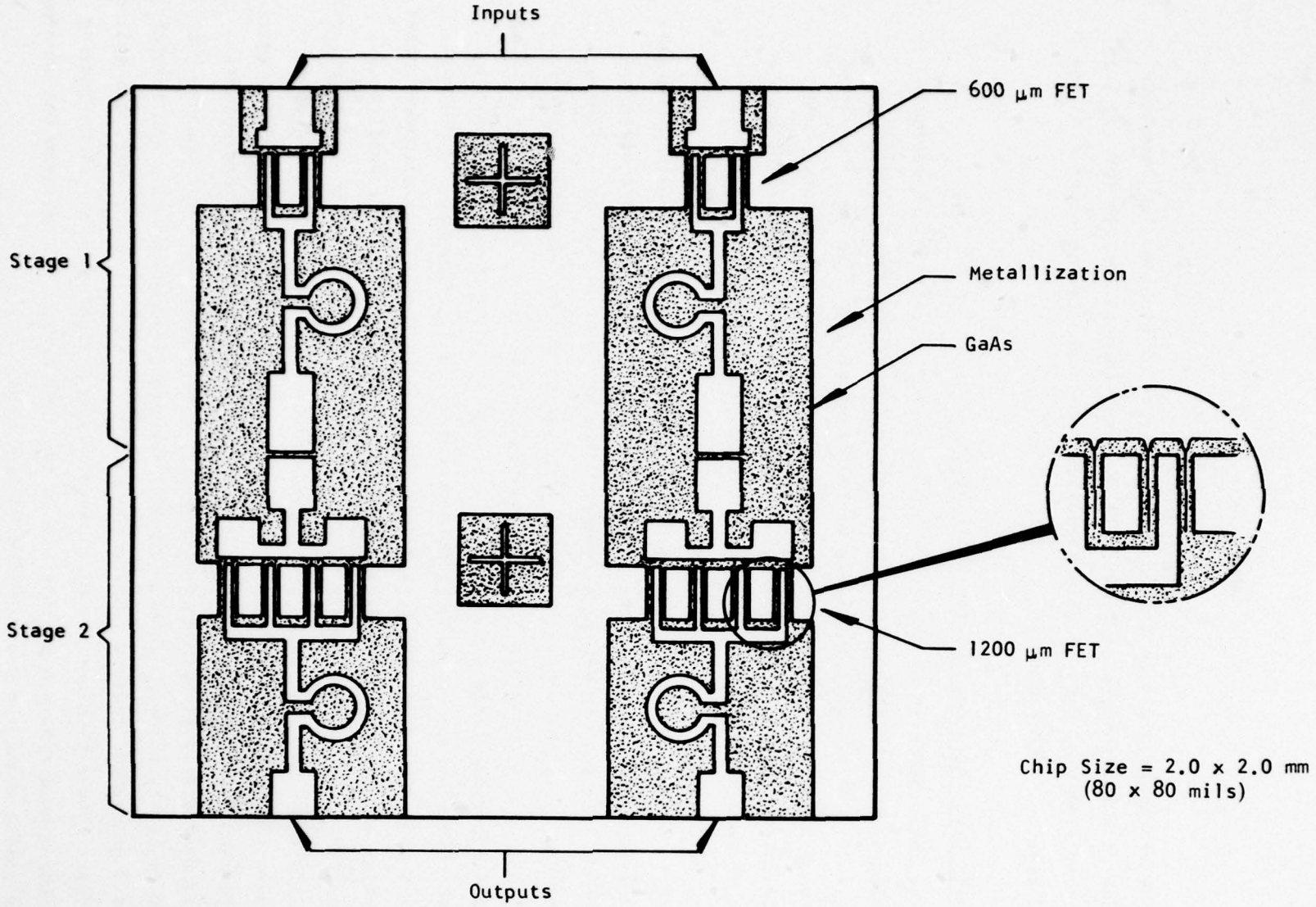


Figure 18 Two-Stage Push-Pull Monolithic Power Amplifier

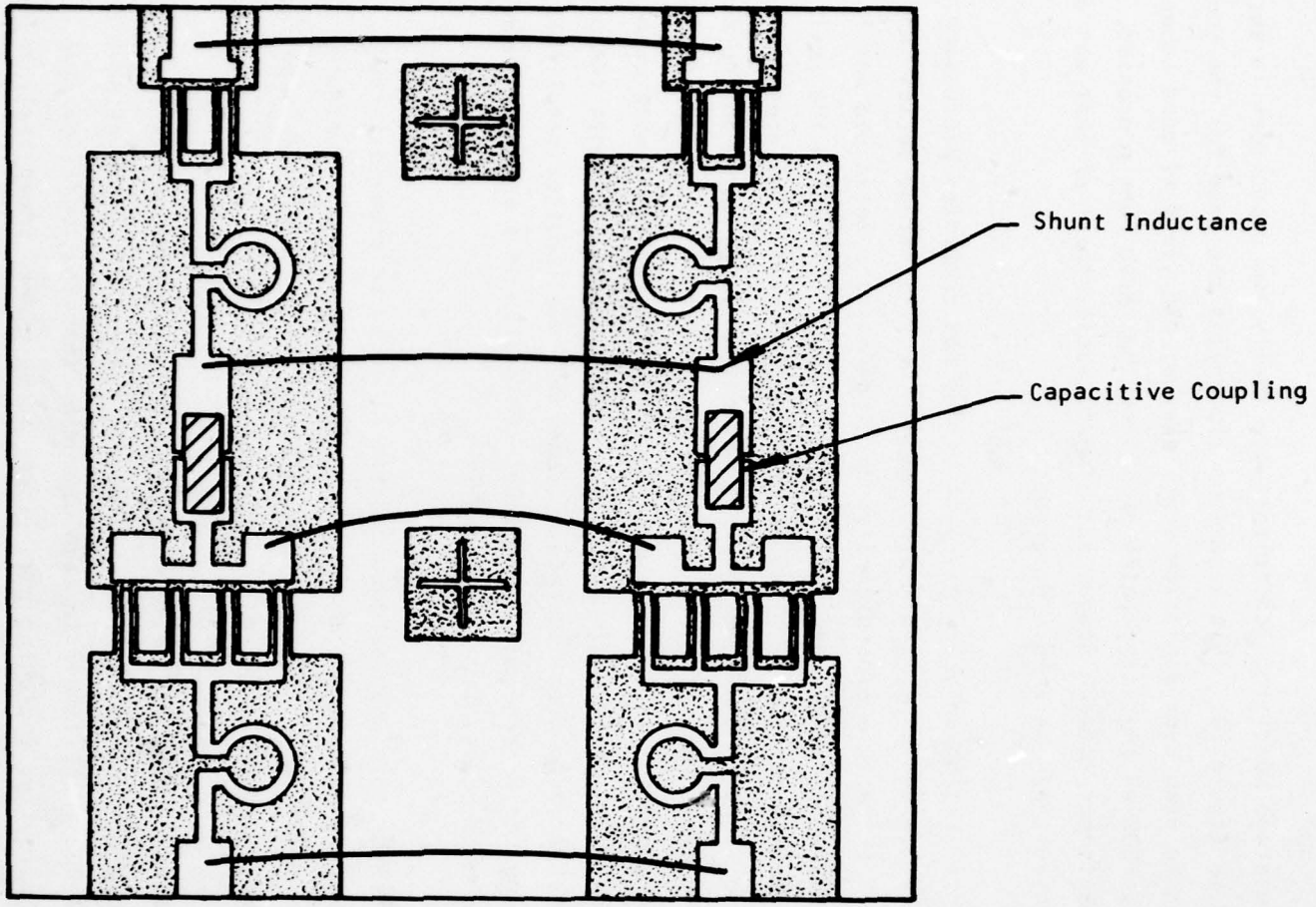


Figure 19 Location of Capacitive and Shunt Inductive Elements

The interstage monolithic capacitors are really two capacitors in series as indicated in Figure 20. This technique eliminates the need for the top metallization to step over a nitride edge. Hence, the yield of good capacitors was virtually 100% on the first batch of slices that have been processed. The measured capacitance between stages was almost exactly the 1 pF that was desired, and breakdown voltages were 18 V or greater.

As of this writing only one group of slices has completed processing. The yield was very low due to lift-off problems at the first-stage series inductor. This inductor is nearly a closed circle, and the interior metal did not lift off on most devices. Hence, we initiated a technique [6] in which the resist is soaked in benzene after exposure and prior to development. This results in a resist profile in which the lower part of the resist is undercut during development. This greatly improved the lift-off problem. We plan to further improve the problem by generating a new series inductor mask in which the circle is more open and a dot is placed in its center. In any event, tape was used to remove the original defective metallization with moderate success, and the inductor metallization was reapplied using the benzene soak technique. This allowed a moderate number of amplifiers to be successfully fabricated.

The amplifier chip was designed so that it could be cleaved in half, thereby producing a separate stage 1 and stage 2. This allows initial characterization of each stage separately. Figure 21 shows pictures of a completed amplifier chip and a chip that has been cleaved into two stages.

The amplifier chips are soldered to gold plated copper blocks that can be inserted into a test circuit fixture. The top surface of the mounting block is only 50 μm (0.002 inch) larger in each dimension than the amplifier chip. This enables test circuity, including bias lines, to be placed immediately adjacent to each side of the chip. There are also similar mounting blocks that are half as wide for mounting the cleaved stages. The mounting problems that were experienced

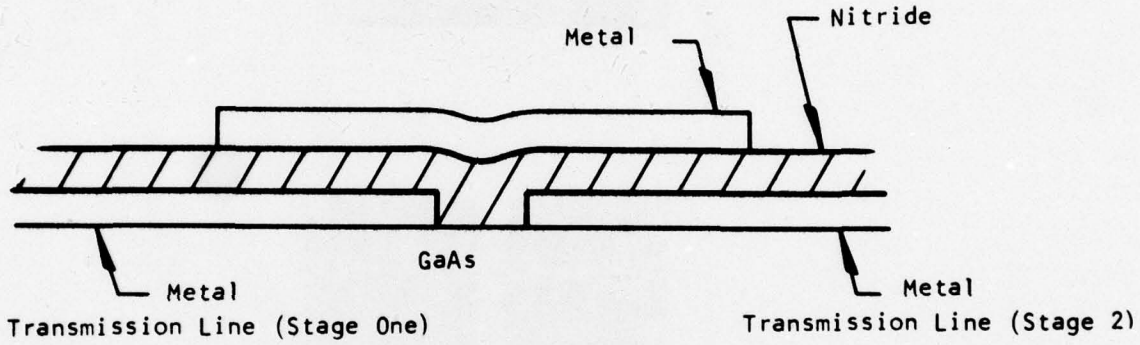
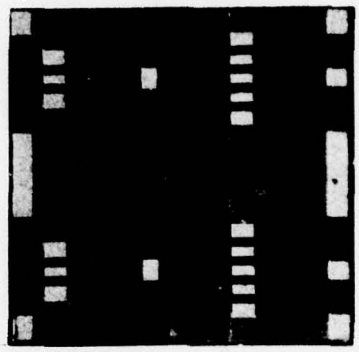


Figure 20 Interstage Monolithic Capacitor, (Essentially Two Capacitors in Series)

(a)



(b)

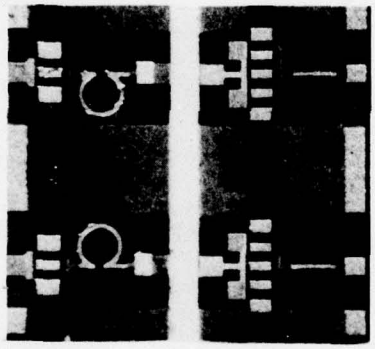


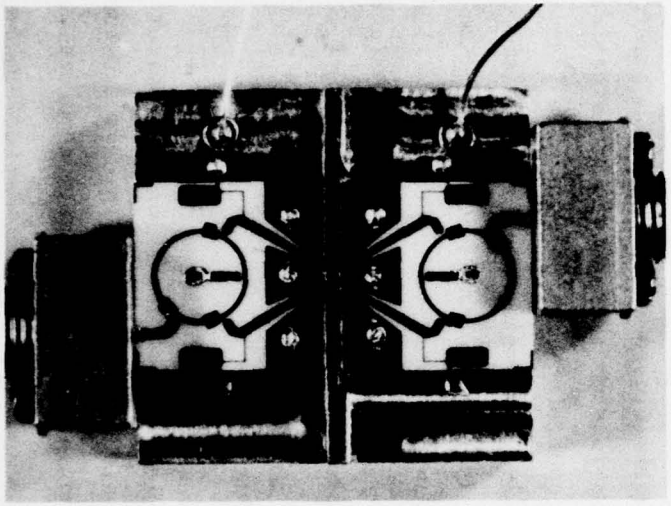
Figure 21(a) Two Stage Monolithic Push-pull Power Amplifier Chip
(b) The Amplifier Chip Cleaved into Stage One and Two to Allow Separate Characterization of Each Stage

in the early part of the program have been alleviated. These occurred because the normal mounting procedure for discrete devices (holding the device in tweezers and scrubbing it back and forth on the mounting block assure good solder contact) was inappropriate for the larger, more fragile monolithic chips. Hence, flux was used to assure even solder spreading and adhesion. Any excess flux is then removed in hot water. This technique was used to mount several discrete devices; no changes in dc or microwave characteristics were caused by the use of the flux.

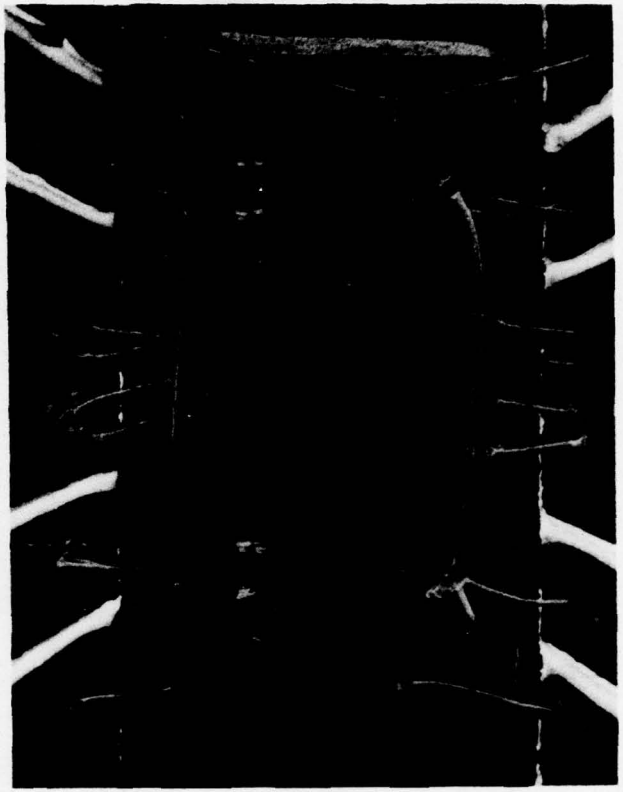
C. Push-Pull Amplifier Results - First Stage

Prior to testing of the two-stage amplifier the first fabricated devices were sawed in half for testing of the first stage. To obtain maximum gain from the first stage when connected to the nominally 50 Ω interface circuits, a somewhat different tuning is required on the output of the 600 μm FET devices as compared to the case when the second stage is present. This tuning change can be realized by changing the output shunt inductance element, as shown in Figure 22. Figure 22(a) shows the total amplifier, while Figure 22(b) is an SEM enlargement of the monolithic device. Ideally, connections to the chip from the device need to be as short as possible. Grounding connections can be made with fine gold mesh, but in the photo of Figure 22 several 25 μm diameter bonding wires are used instead. Figure 22(b) shows the two series inductors monolithically integrated on the chip. Coplanar ground metallization is in the center, as well as on both edges of the 1 mm x 2 mm GaAs chip. Figure 23 shows the small signal gain of the amplifier in Figure 22(a). The gain includes the approximately 0.8 dB loss through both 180° hybrid rings. At 9.5 GHz a small-signal gain of 8 dB is observed. The 1 dB fractional bandwidth is 10%.

To test the amplifier under large signal conditions the output shunt wire was lengthened by about 40% to compensate for the change in device output impedance at large-signal levels. Figure 24 shows the resulting gain compression characteristic



(a)



(b)

Figure 22 Monolithic Push-Pull Amplifier at 9.5 GHz
(a) Overall Amplifier
(b) SEM Photo of Device Details

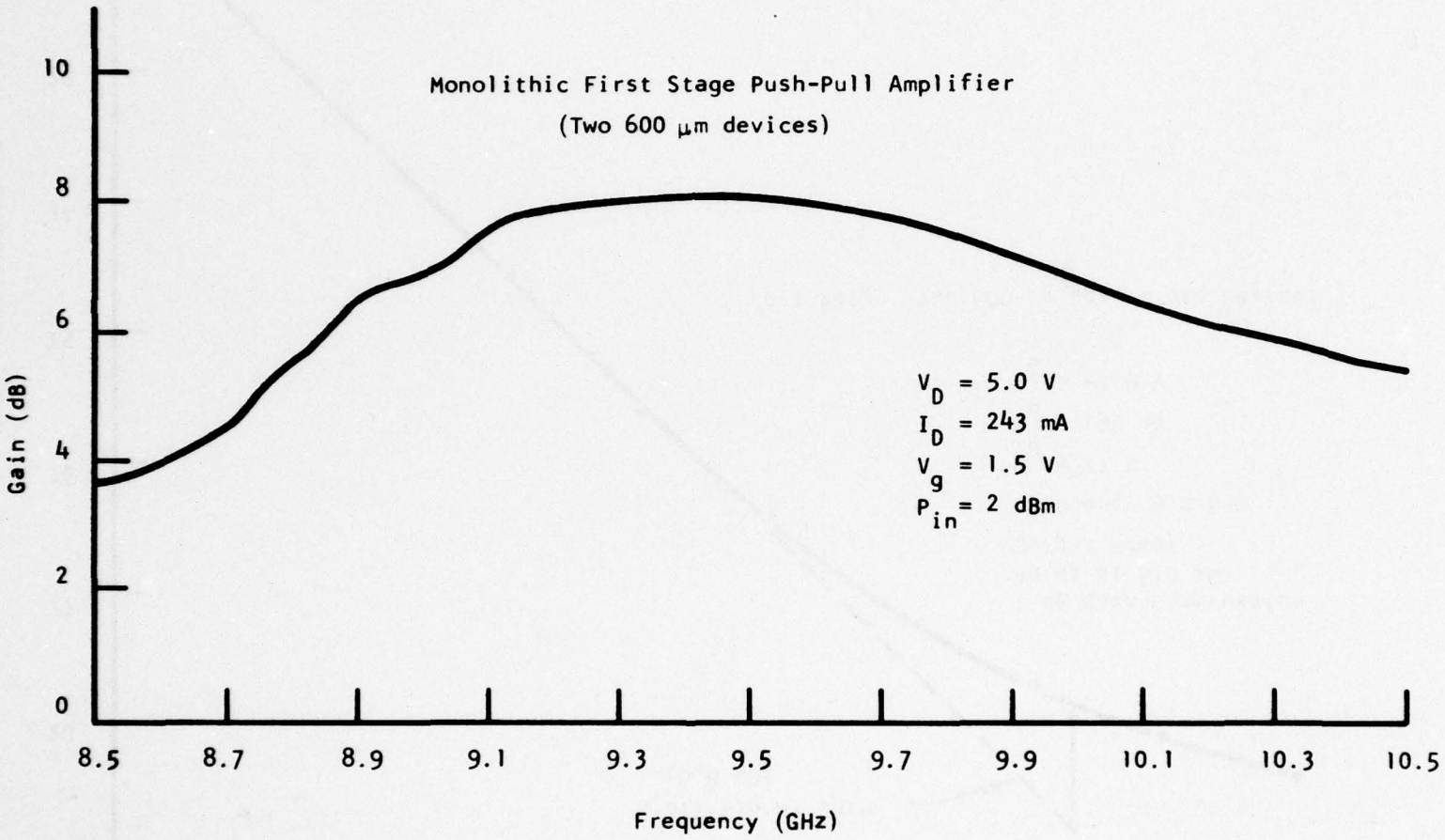


Figure 23 Small Signal Gain of Amplifier Shown in Figure 22

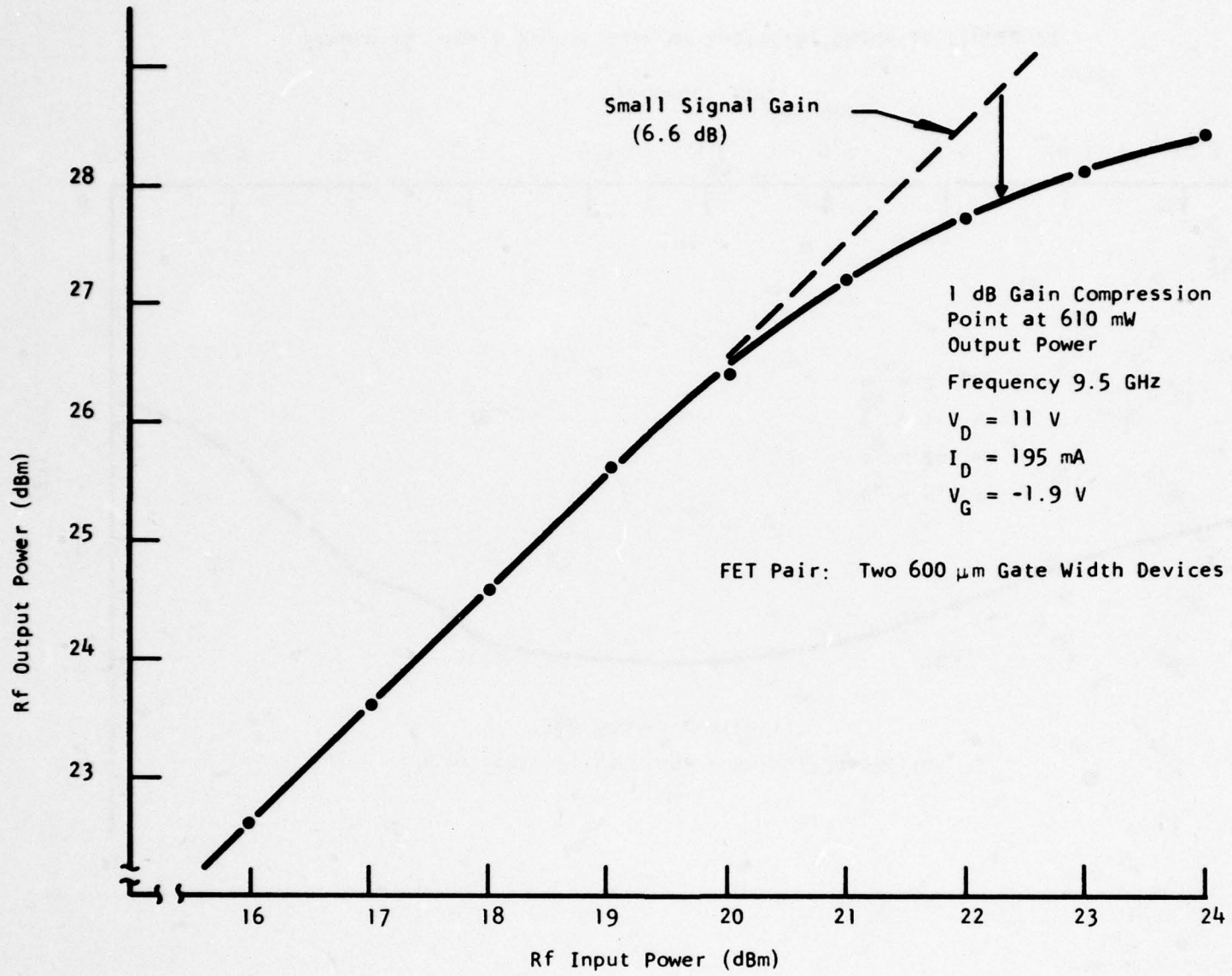


Figure 24 Gain Compression Curve for Retuned Amplifier of Figure 22

for this amplifier at 9.5 GHz. A small signal gain of 6.6 dB (from OSM connector to connector) and a 1 dB gain compression point of 27.8 dBm was observed at a drain voltage of 11 V and a drain current of 195 mA. An output power of 28.4 dBm (690 mW) with a gain of 4.4 dB is achieved with this amplifier at 11 V drain bias. At 12 V bias, with the same tuning, the amplifier yielded 28.8 dBm (758 mW) with 4.8 dB gain and a power-added efficiency of 21%.

SECTION IV
SUMMARY OF PHASE I AND PLANS FOR FUTURE WORK

To date, work on the monolithic GaAs Power FET program has included the design of two device mask sets; fabrication and characterization of devices from the first mask set; fabrication and preliminary evaluation of devices from the second mask set; development of passive interface circuits on alumina; and the monolithic realization of an 8 dB, small-signal gain, push-pull amplifier at 9.5 GHz. This amplifier yielded an output power of 28.8 dB (758 mW) with 4.7 dB gain also at 9.5 GHz utilizing the first stage (a pair of 600 μm FETs) of the two-stage monolithic amplifier from the second mask set design.

The second mask set has been designed specifically to realize a two-stage push-pull amplifier. The design includes four transistors, two with 600 μm total gate width and two with 1200 μm total gate width. Emphasis in the mask development was placed on design flexibility. Monolithic series inductors are defined on separate masks, allowing variation of impedance matching elements. A series capacitor fabricated monolithically provides dc blocking between stages. Shunt inductors between the two transistors provide common bias, as well. Initially, the shunt inductors will use 1 mil wires for circuit optimization; subsequently, monolithic integration will be employed. The chip dimensions are 2.0 mm x 2.0 mm x $\sim$ 0.1 mm. A 1.5 W, 10 dB gain, push-pull amplifier is anticipated after evaluation of the entire two-stage device.

To continue the monolithic GaAs power FET work into the second phase, a plan for a one-year program continuation has been developed that will be a natural extension of Phase I and that will lead to a more sophisticated level of monolithic integration of GaAs FET power devices.

The second phase will begin by completing the characterization and optimization of the two-stage, monolithic, push-pull amplifier developed during the first

phase of the program. Power output, gain, bandwidth, third-order intermodulation distortion, AM to PM conversion, and phase linearity will be measured. Circuit optimization will initially be made for maximum output power. Further characterization will allow optimization for other parameters, for example, bandwidth. This work will be done during the first three months of the second phase. The remaining part of the second phase (nine months) will be devoted to the development of an X-band paraphase amplifier consisting of a three-transistor power GaAs FET integrated circuit.

The objective of the paraphase amplifier development will be to replace the passive interface circuits (used to obtain two 180° out-of-phase signals) with an active, unbalanced-to-balanced transformer. Initially, a mask set will be designed for the paraphase amplifier only, to be incorporated later with the input to the push-pull amplifier. Since the first stage of the push-pull amplifier employs two 600 μm gate-width FETs, it is anticipated that the paraphase amplifier will also incorporate comparable gate-width devices. The design of the paraphase amplifier consists of a source-coupled differential pair of FETs, one of whose input gates is grounded, and a current source composed of a single FET whose gate input is held constant at a dc value. By driving the ungrounded gate of the differential pair, a balanced push-pull output is obtained. The key technical problems to be addressed for this development are (1) bias distribution to the three transistors and (2) the design of the current source.

REFERENCES

1. C. P. Wen, "Coplanar Waveguide: A Surface Strip Transmission Line Suitable for Nonreciprocal Gyromagnetic Device Applications," IEEE Trans. Microwave Theory Tech. MTT-17, 1087 (1969).

2. H. M. Macksey and R. L. Adams, "Fabrication Processes for GaAs Power FETs," Proceedings of 1975 Cornell Conference on Active Semiconductor Devices for Microwaves and Integrated Optics, pp. 255-264, August 1975.

3. R. Pucel, D. Masse, and C. Hartwig, "Losses in Microstrip," IEEE Trans. Microwave Theory Tech. MTT-16, 342 (1968).

4. R. E. DeBrecht, "Coplanar Balun Circuits for GaAs FET High-Power Push-Pull Amplifiers," IEEE, 1973 International Microwave Symposium, pp. 309-311.

5. H. Q. Tserng, V. Sokolov, H. M. Macksey, and W. R. Wisseman, "Microwave Power GaAs FET Amplifiers," IEEE Trans. Microwave Theory Tech. MTT-24, 936 (1976).

6. B. J. Canavello, M. Hatzakis, and J. M. Shaw, "Process for Obtaining Undercutting of Photoresist to Facilitate Lift Off," IBM Tech. Disclosure Bull. 19, 4048 (1977).

DISTRIBUTION LIST

TECHNICAL REPORTS

Contract N00014-77-C-0657

Code 427 — 4
Office of Naval Research
Arlington, VA 22217

Naval Research Laboratory
4555 Overlook Avenue, S. W.
Washington, D.C. 20375
Code 5211 — 1
Code 5250 — 1

Defense Documentation Center — 12
Building 5, Cameron Station
Alexandria, VA 22314

Dr. Y. S. Park — 1
AFAL/DHR
Building 450
Wright-Patterson AFB, OH 45433

ERADCOM — 1
DELET-M
Fort Monmouth, N.J. 07703

Texas Instruments — 1
M.S. 105/W. Wisseman
P. O. Box 5936
Dallas, Texas 75222

Commanding Officer — 1
Office of Naval Research
Branch Office
1030 East Green Street
Pasadena, CA 91101

Mr. H. Cooke — 1
Avantek, Inc.
3175 Bowers Avenue
Santa Clara, CA 95051

Dr. R. Bell, K 101 — 1
Varian Associates
611 Hansen Way
Palo Alto, CA 94304

Mr. R. Bierig — 1
Raytheon Company
28 Seyon Street
Waltham, MA 02154

Dr. H. C. Nathanson — 1
Westinghouse Research and
Development Center
Beulah Road
Pittsburgh, PA 15235

Dr. F. Blum/Dr. Daniel Chen — 1
Rockwell International
Science Center
P. O. Box 1085
Thousand Oaks, CA 91360

Mr. G. J. Gilbert — 1
MSC
100 Schoolhouse Road
Somerset, N.J. 08873

Dr. C. Krumm — 1
Hughes Research Laboratory
3011 Malibu Canyon Road
Malibu, CA 90265

Mr. Lothar Wandinger — 1
ECOM/AMSEL/TL/IJ
Fort Monmouth, NJ 07003

Colonel Paul Mosteller — 1
AFOSR/NE, Building 410
Bolling AFB
Washington, DC 20332

Dr. Harry Wieder — 1
Naval Ocean Systems Center
Code 922
271 Catalina Blvd
San Diego, CA 92152

Dr. William Lindley — 1
MIT
Lincoln Laboratory
F124A P. O. Box 73
Lexington, MA 02173

Mr. Sven Roosild — 1
AFCRL/LQD
Hanscom AFB, MA 01731

Commander 1
US Army Electronics Command
V. Gelnovatch
(DRSEL-TL-IC)
Fort Monmouth, NJ 07703

RCA 1
Microwave Technical Center
Dr. F. Sterzer
Princeton, NJ 08540

Hewlett-Packard Corp 1
Dr. Robert Archer
Page Mill Road
Palo Alto, CA 94306

Watkins-Johnson Co. 1
E. J. Crescenzi, Jr./
K. Niclas
3333 Hillview Avenue
Stanford Industrial Park
Palo Alto, CA 94304

Commandant 1
Marine Corps
Scientific Advisor (Code AX)
Washington, D.C. 20380

Communications Transistor Corp. 1
Dr. W. Weisenberger
301 Industrial Way
San Carlos, CA 94070

Microwave Associates 1
Northwest Industrial Park
Drs. F. A. Brand/J. Saloom
Burlington, MA 01803

Commander, AFAL 1
AFAL/DHM
Mr. Richard L. Remski
Wright-Patterson AFB, OH 45433

Professor Walter Ku 1
Phillips Hall
Cornell University
Ithaca, NY 14853

Commander 1
Harry Diamond Laboratories
Mr. Horst W. A. Gerlach
2800 Powder Mill Road
Adelphia, MD 20783

Advisory Group on Electron
Devices 1
201 Varick Street, 9th floor
New York, NY 10014

D. Claxton 1
MS/1414
TRW Systems
One Space Park
Redondo Beach, CA 90278